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CLAIMS

- 1 1. A process of forming a semiconductor structure with a relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer,
2 comprising:
3 depositing a graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer on a first substrate, wherein said Ge
4 concentration x is increased from zero to a value y;
5 depositing a relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer;
6 introducing ions into said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer to define a first heterostructure;
7 bonding said first heterostructure to a second substrate to define a second heterostructure;
8 splitting said second heterostructure in the region of the introduced ions, wherein a top
9 portion of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer remains on said second substrate.
- 1 2. The process of claim 1 further comprising forming at least one device layer or a
2 plurality of integrated circuit devices, after said step of depositing said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer.
- 1 3. The process of claim 2, wherein said at least one device layer comprises at least one of
2 strained Si, strained $\text{Si}_{1-w}\text{Ge}_w$ with $w \neq y$, strained Ge, GaAs, AlAs, ZnSe and InGaP.
- 1 4. The process of claim 1 further comprising forming an insulating layer before said step
2 of introducing ions.
- 1 5. The process of claim 1 further comprising planarizing said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer,
2 before said step of introducing ions.
- 1 6. The process of claim 1, wherein said ions comprise hydrogen H^+ ions or H_2^+ ions.
- 1 7. The process of claim 1 further comprising planarizing said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer, after

2 said step of introducing ions.

1 8. The process of claim 1 further comprising cleaning both said first heterostructure and
2 said second substrate, before said step of bonding.

1 9. The process of claim 1, wherein said second heterostructure is split by annealing.

1 10. The process of claim 1, wherein said second heterostructure is split by annealing
2 followed by mechanical force.

1 11. The process of claim 1 further comprising removing the top portion of the remaining
2 of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer, after said step of splitting.

1 12. The process of claim 1 further comprising forming at least one device layer, or a
2 plurality of integrated circuit devices, after said step of splitting.

1 13. The process of claim 12, wherein said at least one device layer comprises at least one
2 of relaxed $\text{Si}_{1-y}\text{Ge}_y$, strained Si, strained $\text{Si}_{1-w}\text{Ge}_w$, strained Ge, GaAs, AlAs, ZnSe and InGaP.

1 14. The process of claim 1 further comprising re-using the remaining first
2 heterostructure, after said step of splitting.

1 15. The process of claim 1, wherein said first substrate comprises monocrystalline
2 silicon.

1 16. A process of forming a semiconductor layer, comprising:
2 depositing a graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer on a first substrate, said Ge concentration x
3 being increased from zero to 1;

4 depositing a relaxed Ge layer;
5 forming a monocrystalline semiconductor layer including another material whose lattice
6 constant is approximately close to that of Ge;
7 introducing ions into said semiconductor layer to define a first heterostructure;
8 bonding said first heterostructure to a second substrate to define a second heterostructure;
9 splitting said second heterostructure in the region of introduced ions, wherein a
10 top portion of said semiconductor layer remains on said second substrate.

1 17. The process of claim 16, wherein said semiconductor layer comprises one of GaAs,
2 AlAs, ZnSe and InGaP.

1 18. The process of claim 16 further comprising forming at least one device layer or a
2 plurality of integrated circuit devices, after said step of forming said semiconductor layer.

1 19. The process of claim 16 further comprising forming an insulating layer before said
2 step of introducing ions.

1 20. The process of claim 16 further comprising planarizing said semiconductor layer
2 before said step of introducing ions.

1 21. The process of claim 16, wherein said ions comprise hydrogen H^+ ions or H_2^+ ions.

1 22. The process of claim 16, further comprising the step of planarizing said
2 semiconductor layer after said step of introducing ions.

1 23. The process of claim 16 further comprising cleaning both said first heterostructure
2 and said second substrate, before said step of bonding.

1 24. The process of claim 16, wherein said second heterostructure is split by annealing.

1 25. The process of claim 16, wherein said second heterostructure is split by annealing
2 and followed by mechanical force.

1 26. The process of claim 16 further comprising removing the top portion of the
2 remaining of said third semiconductor layer, after said step of splitting.

1 27. The process of claim 16 further comprising forming at least one device layer or a
2 plurality of integrated circuit devices, after said step of splitting.

1 28. The process of claim 16 further comprising re-using the remaining first
2 heterostructure, after said step of splitting.

1 29. The process of claim 16, wherein said first substrate comprises monocrystalline
2 silicon.

1 30. A process of forming a semiconductor structure with a relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer,
2 comprising:

3 depositing a graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer on a first substrate, said Ge concentration x
4 being increased from zero to a selected value y, and y being less than 0.2;

5 depositing a relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer, where z is between 0.2 and 0.25;

6 introducing ions into said graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer to define a first heterostructure;

7 bonding said first heterostructure to a second substrate to define a second heterostructure;

8 splitting said second heterostructure in the region of introduced ions, wherein the upper

9 portion of first graded $\text{Si}_{1-x}\text{Ge}_x$ layer and said relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer remains on said second

10 substrate; and

11 selectively etching the remaining portion of said graded $\text{Si}_{1-x}\text{Ge}_x$ layer, wherein
12 said relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer remains on said second substrate.

1 31. The process of claim 30 further comprising forming at least one device layer or a
2 plurality of integrated circuit devices, after said step of forming said relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer.

1 32. The process of claim 31, wherein said at least one device layer includes one or more
2 of strained Si, strained $\text{Si}_{1-w}\text{Ge}_w$ with $w \neq z$, and strained Ge.

1 33. The process of claim 30 further comprising forming an insulating layer before said
2 step of introducing ions.

1 34. The process of claim 30 further comprising planarizing said relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer
2 before said step of introducing ions.

1 35. The process of claim 30, wherein said ions comprise hydrogen H^+ ions or H_2^+ ions.

1 36. The process of claim 30 further comprising planarizing the relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer
2 after said step of introducing ions.

1 37. The process of claim 30 further comprising cleaning both said first heterostructure
2 and said second substrate, before said step of bonding.

1 38. The process of claim 30, wherein said second heterostructure is split by annealing.

1 39. The process of claim 30 further comprising planarizing said second relaxed $\text{Si}_{1-z}\text{Ge}_z$
2 layer after said step of etching.

1 40. The process of claim 30 further comprising forming at least one device layer or a
2 plurality of integrated circuit devices, after said step of etching.

1 41. A process of forming a semiconductor layer, comprising:
2 depositing a graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer on a first substrate, said Ge concentration x
3 being increased from zero to a value y ;
4 depositing a relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer;
5 depositing a strained or defect layer;
6 depositing a relaxed layer;
7 introducing ions into said strained or defect layer to define a first heterostructure;
8 bonding said first heterostructure to a second substrate to define a second heterostructure;
9 and
10 splitting said second heterostructure in the region of the strained or defect layer,
11 wherein said relaxed layer remains on said second substrate.

1 42. The process of claim 41, wherein said strained or defect layer comprises either a
2 strained $\text{Si}_{1-z}\text{Ge}_z$ layer with $z \neq y$, or other III-V material.

1 43. The process of claim 41, wherein said relaxed layer or said strained or defect layer
2 comprises either a relaxed $\text{Si}_{1-w}\text{Ge}_w$ layer where w is close or equal to y , or, when y is equal to 1,
3 one of Ge, GaAs, AlAs, ZnSe and InGaP.

1 44. The process of claim 41 further comprising forming at least one device layer or a
2 plurality of integrated circuit devices, after said step of depositing said relaxed layer.

1 45. The process of claim 41 further comprising forming an insulating layer before said
2 step of introducing ions.

1 46. The process of claim 41 further comprising planarizing said relaxed layer before said
2 step of introducing ions.

1 47. The process of claim 41, wherein said ions comprise hydrogen H^+ ions or H_2^+ ions.

1 48. The process of claim 41 further comprising planarizing said relaxed layer after said
2 step of introducing ions.

1 49. The process of claim 41 further comprising cleaning both said first heterostructure
2 and said second substrate, before said step of bonding.

1 50. The process of claim 41, wherein said second heterostructure is split by annealing.

1 51. The process of claim 41 further comprising removing one of any remaining of said
2 strained or defect layer, and the top portion of said relaxed layer, after said step of splitting.

1 52. The process of claim 41 further comprising forming at least one device layer or a
2 plurality of integrated circuit devices, after said step of splitting.

1 53. The process of claim 41 further comprising re-using the remaining first
2 heterostructure for a subsequent process after planarizing.

1 54. A semiconductor structure comprising:
2 a first semiconductor substrate;
3 a second layer of relaxed $Si_{1-x}Ge_x$, wherein $x = 0.1$ to 1 ; and

4 a third layer comprising at least one of GaAs, AlAs, ZnSe and InGaP, or strained $\text{Si}_{1-y}\text{Ge}_y$,
5 wherein $y \neq x$.

1 55. A semiconductor structure comprising:
2 a first substrate comprising monocrystalline silicon substrate;
3 a second layer of graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer, wherein said Ge concentration x is
4 increased from zero to a value y ;
5 a third layer of relaxed $\text{Si}_{1-y}\text{Ge}_y$;
6 a fourth strained or defect layer comprising either a strained $\text{Si}_{1-z}\text{Ge}_z$ layer with $z \neq y$, or
7 other III-V or II-VI material; and
8 a fifth relaxed layer comprising either a relaxed $\text{Si}_{1-w}\text{Ge}_w$ layer where w is close or equal
9 to y , or, when y is equal to 1, at least one of Ge, GaAs, AlAs, ZnSe and InGaP.